(FILE 'USPAT' ENTERED AT 15:07:03 ON 12 SEP 96)

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L1          7378 S MEMORY ARRAY#
L2            63 S BUS (A) BRIDGE#
L3             1 S L1 (P) L2
L4             5 S L1 AND L2
L5           256 S BANDWIDTH (P) PERIPHERAL
L6             9 S L2 AND L5
L7           875 S LOAD# (A) STORE#
L8             0 S L2 AND L7
L9            48 S L1 AND L7
=> d cit l6 1-9
```

1. 5,522,050, May 28, 1996, Bus-to-**bus** **bridge** for a multiple bus information handling system that optimizes data transfers between a system bus and a peripheral bus; Nader Amini, et al., 395/306, 182.04 [IMAGE AVAILABLE]

2. 5,519,872, May 21, 1996, Fast address latch with automatic address incrementing; Narendra Khandekar, et al., 395/775, 310, 403 [IMAGE AVAILABLE]

3. 5,499,346, Mar. 12, 1996, Bus-to-**bus** **bridge** for a multiple bus information handling system that optimizes data transfers between a system bus and a peripheral bus; Nader Amini, et al., 395/308; 371/49.1; 395/185.02 [IMAGE AVAILABLE]

4. 5,469,435, Nov. 21, 1995, Bus deadlock avoidance during master split-transactions; William T. Krein, et al., 370/85.2; 395/285, 290, 303, 842 [IMAGE AVAILABLE]

5. 5,467,295, Nov. 14, 1995, Bus arbitration with master unit controlling bus and locking a slave unit that can relinquish bus for other masters while maintaining lock on slave unit; Bruce Young, et al., 395/200.05; 364/242.6, 242.92, 242.94, DIG.1 [IMAGE AVAILABLE]

6. 5,450,551, Sep. 12, 1995, System direct memory access (DMA) support logic for PCI based computer system; Nader Amini, et al., 395/299, 308, 847, 848 [IMAGE AVAILABLE]

7. 5,448,704, Sep. 5, 1995, Method for performing writes of non-contiguous bytes on a PCI bus in a minimum number of write cycles; David G. Spaniol, et al., 395/310; 364/239, 239.1, 239.7, 240, DIG.1; 365/189.05, 221; 395/427, 821 [IMAGE AVAILABLE]